

Low Cost, High Reliability Electroplating WLP Technology Integration of SnAg chip to chip interconnect

A survey of cost effective electroplating lead free bumps

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Biography

Paul Sibley has been with Semitool since 1990 in various capacities, including engineering, advanced packaging division management, product engineering, Cu interconnect and wafer level packaging. Prior to joining Semitool, Sibley spent eleven years at Biola University in Los Angeles, California as a faculty/staff member with a background bio-medical engineering at Pacific Lutheran University in Washington, and computer science at Biola University.

Paul Sibley has held various positions in engineering at Semitool and has been a general manager of the corporate Advanced Packaging Division and was a founding board member of the global advanced packaging consortium SECAP. He is also a board member for the new 3D consortium EMC-3D. Currently Sibley is VP of ElectroChemical Deposition with a focus on electroplating both wafer level packaging and MEMS applications. Sibley is also VP of corporate marketing

Abstract

From 2002 to the present, various methods of using solder bumps to interconnect chip to chip or chip to substrate interconnect using Flip Chip (FC) and Wafer Level Packaging (WLP) have been integrated successfully into production bumping lines. These solder bumps can range in size from 50 to 500 microns and, depending on the application, can be created using electroplating, paste, ball placement or evaporation.¹ In many applications large pitch and bumps (>180um) allow for low cost paste or placement technologies and have proven to be cost effective.

Small diameter bumps (<150um) and fine pitch on large die of 1000 or more I/O per die have been preformed by evaporation or electroplating. This application required changing process steps and tightly controlling uniformity/composition to create high yields and low defects. In order to achieve this, several factors such as under bump

metal (UBM) lithography masking, materials changes and deposition of the bumps needed to be updated with technology commonly found in the front-end wafer fabs.

Although this enabled pitch and bump I/O count that previously wasn't available, it also created an expensive process flow.

Over the years, with the advent of 300mm fabs, and consortiums concentrating on low cost bumping lines, these costs came down to reasonable numbers while maintaining the high yields and technology node. For example, the initial cost base the semiconductor equipment consortium for advanced packaging (SECAP) began working on was a \$310/wafer composite CoO, including all steps from initial clean thru dice. The consortium worked on several high cost steps including lithography, UBM etch, photo-template removal and electroplating in order to make the equipment more efficient and reduce the overall cost of each step. The successful SECAP consortium was disbanded once the technology was widely adopted and the CoO was reduced to under \$130/wafer.²

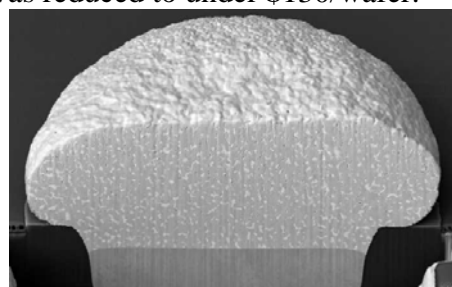


Figure 1: Low Cost SECAP bumping process 2004

The efforts of SECAP reduced the cost of all the individual steps dramatically, while improving the integration and overall yield. For instance, the electroplating step for the 95/5 high lead bump of 100um was reduced from an initial cost of \$18.50/wafer to just under \$4.80/wafer.³ This was done in a combination of breakthrough developments including longer bath life, lower equipment run cost and higher throughput.

Today, many steps of a 95/5 lead(Pb)/tin(Sn) bump are being used in the integration of lead free bumps, replacing the 95Pb/5Sn by a stack of copper, nickel and lead-free. The material choice of stacking metals is used to improve reliability and defects typically found in high tin bumps.

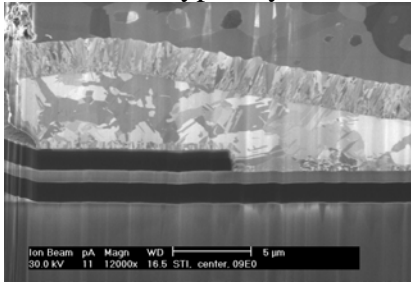


Figure 2: Copper, Nickel, Tin-Silver bump stack

There are three primary issues with changing the proven 95Pb/5Sn material with new lead free bumps such as SnAg;

Issue #1, Reliability of UBM interface: An effort to replace the high cost Cr/CrCu/Cu UBM has been successful creating high yielding bumps. This integration has been successful at various production lines using barrier layers of Ti, TiW, or TiN with a Copper plating base or Seed Layer.⁴

Issue #2, Repeatability of composition control in plated alloys. The composition of the lead free bump is largely being adopted from three different configurations. SnAgCu, SnCu, and SnAg have all been developed to some degree in R&D lines. For this paper, CoO and Reliability numbers used 97.5Sn/2.5Ag for the lead free bump material.

Issue #3, Cost of Ownership of a bumping line using not one plated metal but three. One of the more common structures being integrated into bumping lines is an electroplated compliant stud of 8um copper, a diffusion barrier of 2um electroplated Ni and the lead free bump. The purpose of the nickel is to prevent the copper being absorbed into the high tin bump, which can create a brittle Cu/Sn inter-metallic interface and be a likely failure point in thermal cycling.

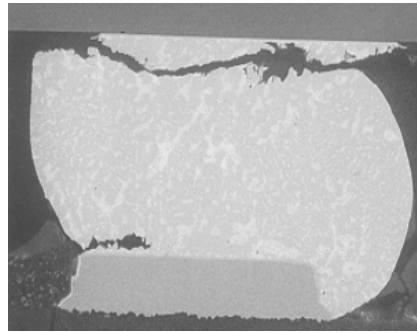


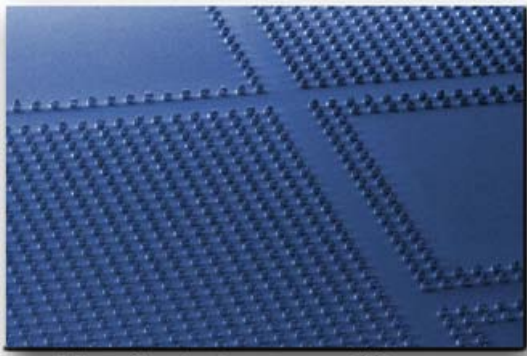
Figure 3, Known failures at the metallic interface, reported by Peter Elenius/Tom Goodman of E&G Technology Partners

This failure has been addressed by adding the Copper stud and Nickel barrier to the structure. Currently 1000hr thermal cycle testing, highly accelerated stress testing (HAST96/168hr), and the temperature humidity stress testing (HTS) 500 and 1000hr all pass.

However, the inclusion of additional layers requires many more process steps to be included in the electroplating equipment. At previous deposition rates in vertical plating equipment or fountain cup electro-plating cells, this would require equipment to have over 8 support processing chambers such as cleaners, drying and pre-wet stations as well as over 15 electroplating stations. These tools would be large, complex requiring automation challenges which drive the cost up.

The estimated CoO for this equipment would be well over \$45.00/wafer for the electroplating step alone. To reduce this cost it is required to plate much faster on smaller equipment that has few moving parts and electroplating cells.

The challenge is to create a reliable lead free bumping line for under \$200/wafer. This requires the electroplating step to be reduced from \$45/wafer to under \$15/wafer for all three metals. To accomplish this, a plating rate of over 7um/minute is required with as few automated cells as possible. This paper outlines the issues and solutions that have enabled this low-cost, high reliability process step.



75um Sn-Ag bumps on 300mm

Figure 4, low-cost/high-reliability stacked lead-free structure.

The following discussion is the result of many years of collaboration and integration that has resulted in a reduced cost lead-free process without sacrificing the yield and reliability.

Data (Technical Solution achieved in production processing low cost Electroplated Lead-Free WLP):

The UBM structure must provide the many different capabilities including adhesion, ionic barriers, metal interface barrier and low resistance plating base. Typically the issues facing the barrier include⁵:

- Adhesion to wafer passivation
- Low ohmic contact to final metal
- Robust solder barrier layer
- Easily removed field metal
- Wettable solder layer
- Protect IC metal from the environment
- Materials consistent with wafer processing
- Minimize stress on silicon
- Ability to be used on probed wafers
- Removal with end-point capability

Using the UBM material of TiN with a copper and nickel-plated base, typically creates a IMC of less than 5um after 1000 hr thermal cycling. The failure mode of shear testing is in the solder, not at the UBM interface.



Figure 5, Shear testing showing failure mode on solder, not at the UBM.

All solder processes create a mixing of barrier layers with interconnect material called a IMC (Inter-metallic-compound) This cannot be avoided but must be reduced. With testing of

reflow data, typical IMC of 1.9 to 3.8um is commonly achieved. This creates an effective barrier over time, and can eliminate the effect of Copper seed inclusion into the interconnect material. Composition control therefore can be a concern of the electroplating step alone. While plating a few wafers at only 1.0 – 2.3um/minute is easily achievable it doesn't address the production requirements.

Electroplating Lead-Free Bump

Several alloy compositions have been attempted. The most feasible choice for overall process integration is SnCu, SnAg and SnAgCu. SnAg process has several advantages over the other processes when considering high volume production. The critical advantage is a longer bath life (in terms of tin oxidation). As copper ions in the bath caused the catalytic oxidation of tin ions, SnCu and SnAgCu baths became very unstable over time.⁶

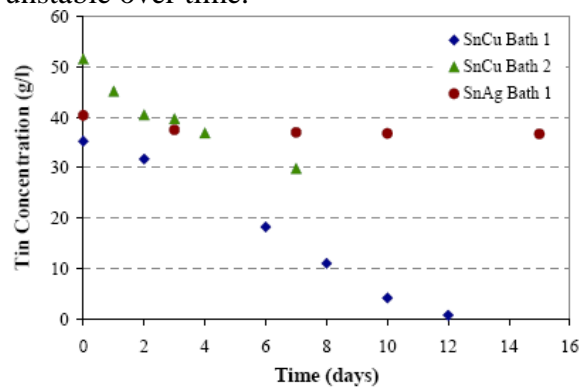


Figure 6. The oxidation of stannous tin in SnCu and SnAg baths over time; solution circulating in a plating chamber at 25°C and 3 gallons per minute (gpm).

The variation of stannous tin concentrations in SnCu and SnAgCu baths over time has proven to be difficult to overcome. The oxidation speed of tin ions in SnCu baths was much faster than in a SnAg bath. As tin ions in the SnAgCu bath were complexed⁶, the lifetime of the SnAgCu bath was better than that of SnCu baths, but was still not comparable to that of the SnAg bath. Other advantages of the SnAg process include relatively easy bath monitoring and maintenance. Tin concentration had no significant influence on alloy composition unless the deposition current density is higher than LCD, and the silver content in deposits was high enough to be measured nondestructively. Besides difficulty in measuring alloy composition, another concern for ternary alloys with small amounts of alloying elements comes from difficulty in controlling and maintaining bath and alloy composition at high

volume production. The composition of ternary alloys is more sensitive to deposition conditions than that of binary alloys. Despite the technical challenges with these lead free baths, several promising chemistries are being used in production and largely have addressed the viability issues. Bumps can now be plated with good composition uniformity.

Composition Uniformity:

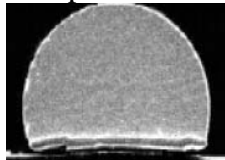


Figure 6, SEM of SnAg bump showing uniform composition.

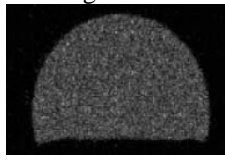


Figure 7, Composition of Sn in reflow bump showing uniform composition.



Figure 8, Composition of Ag in reflow bump showing uniform composition.

Several conflicting issues with the deposition of SnAg for production still exist. High throughput is a requirement, small equipment footprint is a desire and good process control is essential. These contradictory requirements force the user to increase throughput and process controls, or accept complex equipment holding more processing chambers.

Issue #1: Equipment that has high reliability and low consumables and footprint. In order to create a overall CoO of less than \$200/wafer, the electroplating equipment is constrained to be able to run at over 90% uptime, and have a footprint of under 200sq/ft overall. Assuming good process controls and typical cost for the equipment, this would yield an electroplating step of under \$15/wafer. Increase the footprint to 350sq ft increases the CoO to over \$19/wafer, and decreasing the uptime to under 80% typical to large vertical plating cells of over 12 stations. This yields an overall CoO of just above \$32/wafer.

The conclusion that is drawn is the equipment must be designed for reliability typically found in FEOL fabs, fewer than 12 process chambers and

must be smaller than 200sq ft in order to be cost effective.

Issue #2, Composition control at high deposition rates of SnAg. Many problems arose in lead-free solder deposition because alloying elements (such as silver and copper) had significantly higher reduction potentials and lower concentrations than tin. This phenomenon caused several fundamental difficulties and differences from PbSn solder deposition, including a drastic change of morphology and composition with varying current density (or potential).⁸

Despite the challenges, there is substantial interest in lead-free solders. The EU's Waste Electrical and Electronic Equipment (WEEE) and Restriction of Hazardous Substances (RoHS) directives have been driving the adoption of lead-free device application.⁷ Another serious concern for upcoming technology generation is ²¹⁰Pb-created alpha-particle radiation.⁹ The FC interconnects should have minimal levels of alpha-particle radiation to limit soft errors in complementary metal-oxide semiconductor (CMOS) technology. Pure tin is considered one type of lead-free material due to good wettability, better non-toxicity, and ease of deposition. However, even though some researchers showed promising initial results with pure tin,⁷⁻⁹ the use of pure tin has been restricted due to tin whiskers which bridge leads and cause short circuits.^{7,11}

Near-eutectic SnAg polarization behavior

Figure 9 shows typical polarization behavior of a SnAg bath. The initial curve slopes gently and then forms a plateau, corresponding to the potentials where primarily silver ions are deposited.

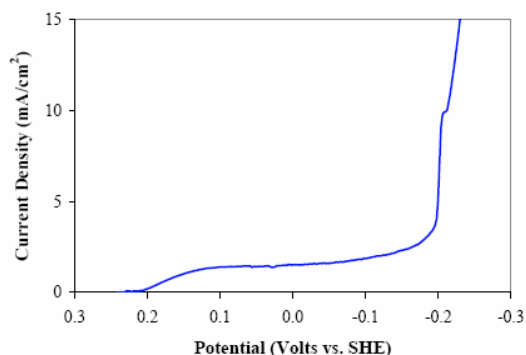


Figure 9, Initial part of SnAg polarization curve showing the first plateau; RDE, room temperature, 1000 revolutions per minute (rpm), and 20mV/sec.

The sharp rises in the curve is related to the deposition potential of tin in the deposit.

Therefore, SnAg alloys are obtained only when the current density is driven beyond the mass transfer limitation of silver ions. The second plateau at higher potentials is caused by the mass transfer limitation of tin ions. The challenge for plating equipment, is to effectively control the as plated composition while increasing the current in order to achieve the targeted >7.0um/minute deposition rate.

Current Density vs. Alloy Composition

As reported at the 205th Meeting of the ECS, Symposium, May 2004, in figure 10, this mass transfer and diffusion-limited process can be understood and compensated by modeling and intelligent design of the electroplating cell. Simple agitation assist but must be accommodated with current density control across the different zones of the wafer. With everything being under control, we can now achieve greater than 7um/minute deposition rate while maintaining control of the composition and uniformity.

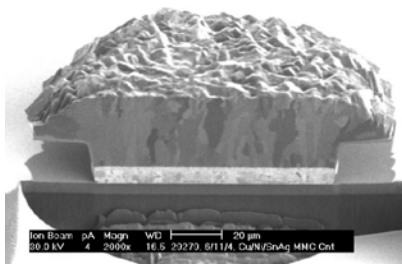
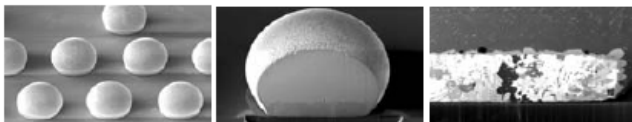


Figure 10, Plated SnAg bump plated at high deposition rates showing good uniformity over a variety of open areas.

Reflow tests, which were performed with the same wafers, showed spherical shapes with smooth surfaces for all cases. No significant differences in reflowability have been found in SnAg samples, SnAgCu or SnCu experiments. The average melting points of the whole bumps in each wafer are found to be 224C; only several degrees off the 221C theoretical eutectic temperature.



(b) Cu/SnAg Solder Stacks

Figure 11, Shows as reflowed SnAg bump of as deposited and FIB to evaluate IMC creation.

Conclusion (CoO targets required for production adoption of Lead-Free WLP can be achieved)

An evaluation of the composite Cost of Ownership (CoO) associated with a lead-free bumping line in the manufacture of microelectronics is a complex study. Breaking out individual steps starting with the most expensive and addressing integration issues at that step is an effective way to reduce the overall CoO for a bumping fab. Therefore a quick study of the CoO model outlines the parameters needed to reduce the cost. As reported earlier several items must be incorporated.

- FEOL Wafer handling automation
- Bath life consistent with PbSn bumping lines
- Reduced equipment complexity
- Deposition rates of over 7um/minute
- Small footprint electroplating equipment.

Achievable costs:

Lead-free Bumping line CoO < \$200.00/wafer
Electroplating Cu/Ni/SnAg < \$15.00/wafer

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