CHARACTERIZATION OF A BATCH HF VAPOR PROCESSOR FOR MEMS RELEASE ETCHING

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ABSTRACT

Fabrication of MEMS devices often includes a "release etch" step wherein a sacrificial oxide layer is removed in order to leave devices free to move. Because device features are so small, surface tension effects often lead to "stiction," where the device may be stuck to adjacent surfaces due to surface tension, friction or electrostatic forces. Consequently, great care must be taken in the release etch in order to avoid the problem of stiction. Processes used to date range from HF vapor to supercritical fluid processing, but most of these utilize single-wafer technology which severely limits throughput when implemented in production. This paper presents data from a batch HF vapor processor. The process has proven capable of performing the release etch in a uniform and repeatable manner without causing stiction and is suited to volume production applications.

INTRODUCTION

MEMS devices are increasing in complexity and are finding numerous applications in industrial and consumer products. One of the critical processing steps for many such devices is the "release etch." In this step, a sacrificial layer is removed from certain regions to allow a range of motion of specific device features. The amount of material to be removed may vary from a few hundred angstroms to several microns. Where the sacrificial or "release layer" is silicon dioxide based, fluorinated chemistries have been applied in order to achieve the release etch. Many of these etching systems are based on a single-wafer configuration, with a relatively low throughput, especially if the release structure requires the removal of several microns of material.

This paper will present characterization data a batch HF vapor etching system and its application for performing MEMS release etching. The data presented will include etch rate, uniformity, repeatability, and metal contamination.

EXPERIMENTAL

The etch process was performed in a Batch HF Vapor Etch Tool manufactured by Semitool, Inc. A simplified flow diagram of the system is shown in Figure 1. The system operates at ambient temperature and pressure and uses a patented HF/alcohol vapor process (1). Vapor generated from a liquid source using an inert carrier gas passed

through a Mass Flow Controller (MFC) into the patented vapor generator (2). The etchant vapor is delivered to a high density polyethylene (HDPE) chamber which can accommodate wafer sizes up to 200mm in diameter and load sizes from 1 to 25 wafers. Wafers are slowly rotated within the process chamber during vapor delivery to help promote vapor distribution and uniformity of etching. While the system can be configured for a variety of process carriers, for the purpose of these experiments a "clamshell" carrier made of HDPE was used. The carrier design is very open to allow vapor access to the wafers with minimal disruption of flow. It also permits processing different wafer sizes with only a carrier change, making the system quite flexible for experimentation or supporting production as a "bridge" tool. The etch process was characterized on 200mm silicon wafers with various films, including thermal oxide (TOX), densified TEOS and silicon nitride. Various patterned structures were used to evaluate undercut and accelerometer devices were processed . Film measurements were made on a Prometrix UV-1050 ellipsometer. IR and visible light microscope inspections as well as SEM evaluations were performed to characterize the undercut and device impact, with electrical testing performed on accelerometer devices to verify and characterize functionality.

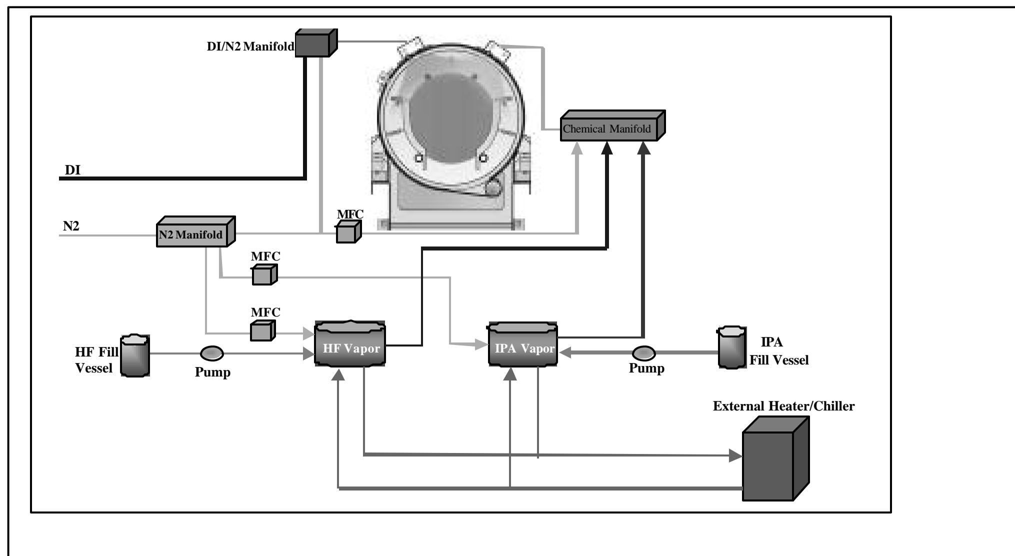

Figure 1: Batch HF Vapor Flow Diagram

RESULTS AND DISCUSSION

Etch Uniformity and Repeatability:

Initial testing on the system was performed using 200mm wafers with 2 microns of thermal oxide on the surface. Film thickness measurements were made on the test wafers using a Prometrix UV-1050 ellipsometer before and after etching, and the etch delta and uniformity ($3\sigma/x$) were calculated. Once the baseline process parameters were defined testing commenced on full 25 wafer loads. We found that within wafer and across load uniformity degraded significantly with full loads of 25 200mm oxide wafers as shown in Figure 2. Poor uniformity was generally characterized by a low oxide etch

rate in the center of the wafers, indicating poor vapor delivery in this region. The erratic etch rate down the load appeared to correspond to the discrete injection points of the vapor into the process chamber.

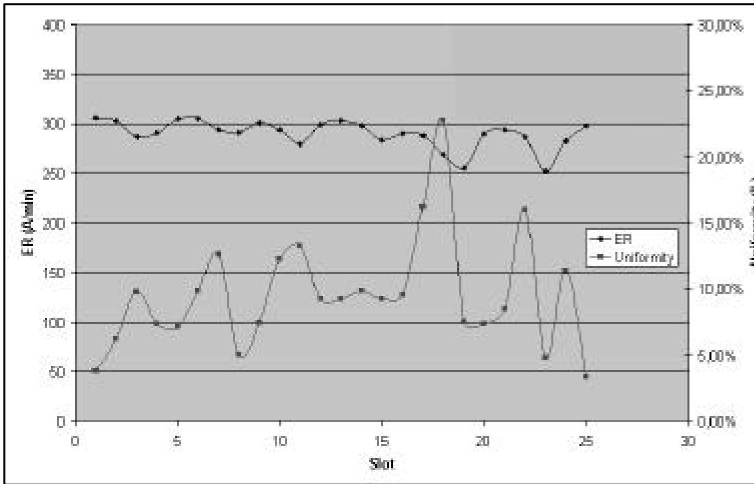

Figure 2: Etch inconsistencies due to oxide loading effect

This had not been observed on 150mm wafers, but was a very pronounced effect on 200mm wafers. However, the degradation did not occur when monitor wafers were processed in full loads of bare silicon wafers. This confirmed that wafer spacing constraining the vapor flow path was not restricting vapor delivery to the center of the monitor wafers. The process degradation was determined to be caused by an oxide loading effect.

Although the vapor flow rate delivered to the process chamber is measured in liters per minute, the actual consumption of HF is on the order of a few milliliters per hour. While silicon dioxide etch using HF is generally considered to be a predominantly rate limited reaction, the vapor phase etch shifts the dynamics into a diffusion limited regime. Our experiments indicate that the chemical reaction is occurring in a condensed film on the wafer surface. As the condensate film forms, the vapor concentration of HF is depleted, resulting in not only a reduction in etch rate as reactants are consumed, but also in a degradation of uniformity as the replenishment of the condensate film is reduced by the depletion of the condensable species. Consequently, one must either increase the amount of vapor – and particularly the condensable species within the vapor stream, or reduce the surface area on which the condensed phase is most likely to form. The condensed phase will preferentially form on the most hydrophilic surfaces. While the presence of the IPA helps to offset this preference, the amount of IPA must still be limited or excessive condensate may form which will lead to problems with stiction. While the 8835 cm^2 of exposed oxide on a batch of 150mm wafers did not pose a problem, the 15707 cm^2 of oxide on a batch of 200mm wafers was more than a single HF vapor generator could etch without experiencing degradation of both the etch rate and uniformity.

We had the option of installing a second HF vapor generator, we decided to not do so. In the first place, time constraints had to be considered. More importantly, the process application for which the system is initially intended will perform a release etch on structures from which the bulk oxide had been previously removed. Consequently, no

oxide is present on the back of the wafers, and only a small percentage of the front surface is covered by the device structure which will be undercut. Thus, the amount of available oxide to be etched is estimated at less than 785 cm^2 in a 25 wafer load. However, characterization was performed on load sizes of 13 wafers having 8168cm^2 of exposed oxide – which is more than 10X the estimated amount exposed on the device wafers. Some test runs were performed on loads having wafers single-spaced, others were run double spaced and some were run with bare silicon wafers in between. The amount of oxide was the critical factor in etch degradation, and no degradation was seen on loads up to 13 wafers with oxide on both front and back regardless of the loading configuration. Etch rate, repeatability and uniformity is shown in Figure 3. Etch data was collected on a Prometrix UV-1050 ellipsometer, measuring 9 points per wafer with a 6mm edge exclusion.

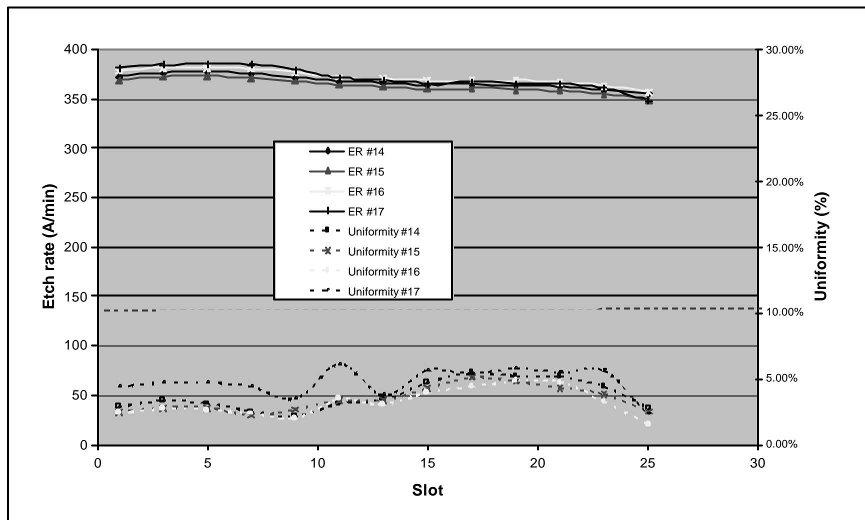

Figure 3: Etch rate repeatability and uniformity without oxide loading effect

While some down the load degradation was observed (less than 5%, 3σ), it was very consistent and a planned hardware modification is anticipated to improve this, and the installation of a second HF vapor generator should also permit etching 25 wafer loads of 200mm wafers without the loading effect noted initially.

Metal Ion Contamination:

Metals analysis was performed on silicon wafers which were exposed to the vapor etch process for an extended period of time. VPD ICP-MS analysis was performed on a control sample and the etched sample in order to determine the impact of the HF vapor processing on metal ion contamination. This data is presented in Figure 4.

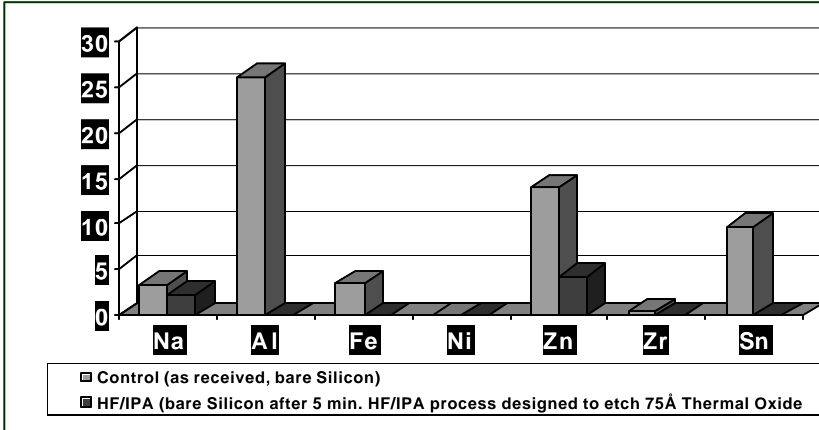

Figure 4: Vapor Phase Decomposition (VPD) ICP-MS concentration in 10^{10} atoms/cm^2

The relatively passive means of generating the vapor seems to effectively prevent metallic contaminants from transitioning from the liquid source into the vapor phase. What was somewhat surprising was the apparent reduction in metal contamination on the wafer surface. None of the elements for which the analysis was performed forms a volatile fluoride. As water rinsing is not part of the process, we are at a loss to propose a mechanism for the apparent reduction in metal ion contamination. It may be that VPD ICP-MS analysis on the hydrophobic surface generated in the vapor etch process is not be an appropriate method for accumulating and analyzing metal contamination.

Particulate Contamination:

Although MEMS devices are generally not considered to be as sensitive to particle contamination as some IC devices, the small geometries and the need to be able to move freely still requires an essentially particle free surface. Particle characterization of the HF/IPA vapor etch process was conducted on wafers having either a native/chemical oxide or a thermal oxide surface. A Tencor Surfscan 6200 particle measurement system was used, and wafers were etched down to the bare silicon surface, often with excessive over-etch to duplicate the process times of the release etch. Results are shown in Figure 5.

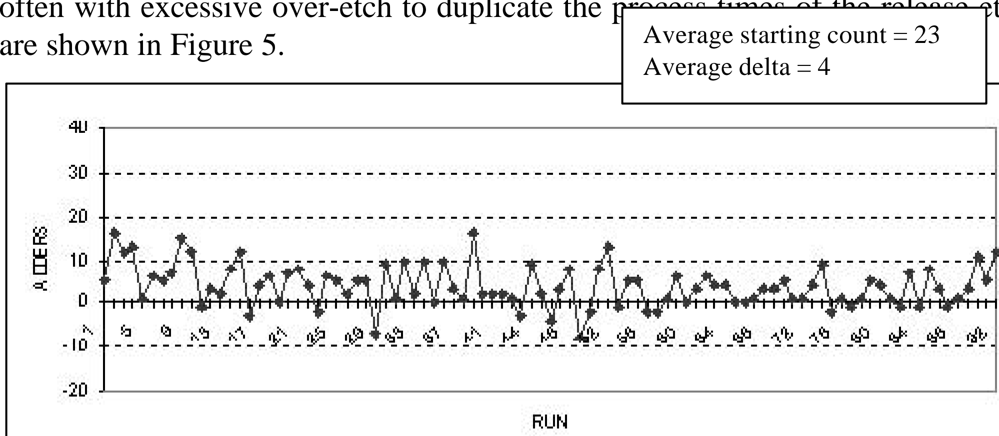

Figure 5: HF vapor particle data (0.2 micron)

The same factors which help to minimize the transfer of metal ion contamination to the wafer surface are thought to also be beneficial in regards to eliminating or minimizing particle transport phenomena. Wafer rotation is always performed at low speed, thereby minimizing turbulence in the process chamber. Gas flows are relatively low in volume, especially during the etch itself. As no process liquids are delivered to the wafer surface, that means of particle transport is eliminated. The vapor is delivered by means of a filtered carrier gas, typically N_2, and the gas stream is filtered to 0.03 microns or better just prior to delivery to the vapor generator. Particle contaminants in the liquid do not readily transition to the vapor due to the passive nature of the vapor generation. All this combines to produce an inherently clean process. The main factor that affects the particle count is the formation of the condensate layer. Formation of a visible condensate film may lead to the formation of water/chemical spots. While not actually particles, they may still have adverse effects on device characteristics. Controlling the etch rate during the surface transition from the hydrophilic to the hydrophobic state is critical in this regard.

Etch Selectivity Between Silicon dioxide and Other Films:

Etch selectivity must be considered when processing devices with different types of exposed films. While our focus is on devices using silicon dioxide as the release layer, there are various dopant species which may be introduced into the oxide film. In addition, materials such as silicon nitride and polysilicon are often present, as well as metals such as aluminum and gold.

The HF/IPA vapor composition can be formulated to provide an etch rate viable for MEMS release etching, typically with an etch rate in the range of 300 - 500Å/minute on thermal oxide. An annealed or densified TEOS oxide exhibits etching behavior similar to that of thermal oxide. However, doped silicon dioxide such as PSG will typically have a much faster etch rate. Regardless of the etch rate, doped silicon dioxide (PSG, BPSG, BSG) are not considered compatible with HF vapor etching because the dopant species will not transition into the vapor phase and will therefore accumulate on the wafer surface. More importantly, species such as phosphorous will react with HF to form a phosphorous or phosphoric acid, which appears as an oily liquid residue on the wafer surface. This acidic residue is not volatile even at temperatures up to 180C, so the most feasible means of removal is to perform a water rinse. However, performing the water rinse after the vapor etch essentially defeats the purpose of performing the vapor etch in the first place, as the displacement of water must be achieved in some means that will not lead to stiction on the devices.

Silicon nitride is etched in the HF vapor process, but the etch rate is highly dependent on they specific nature of the nitride film. In one process, we defined a determined the etch rate on a densified TEOS oxide at 461Å/minute. In the same process we have seen a stoichiometric silicon nitride (Si_3N_4) etch at a rate of 10.8Å/minute for a selectivity of 42:1. However, a silicon rich SiN film showed an etch rate of only 0.8Å/minute, for a selectivity of 576:1. Polysilicon has not shown any attack even after 24 hours of etching.

Metals such as gold or aluminum may also be present on the device surface at the time the release etch is performed. Gold is essentially impervious to attack by HF. Aluminum shows good resistance to the HF/IPA vapor etch, but on occasion we have seen some discoloration of the aluminum surface. This has not been an issue with processes up to 12 hours duration, but we are still attempting to fully characterize the type and extent of attack on aluminum films.

Undercut:

Conventional etch rate tests measure oxide removal in the horizontal plane of the wafer surface. However, the MEMS release etch is required to etch in the vertical plane in order to undercut structures and free them for movement. In order to evaluate the progression of the lateral etch, test structures consisting of ten micron slots etched in a polysilicon layer over a one micron thermal oxide film were prepared. These structures were etched for progressively longer periods of time and the amount of undercut was measured under an IR microscope. The results of this series of tests are depicted in Figure 6.

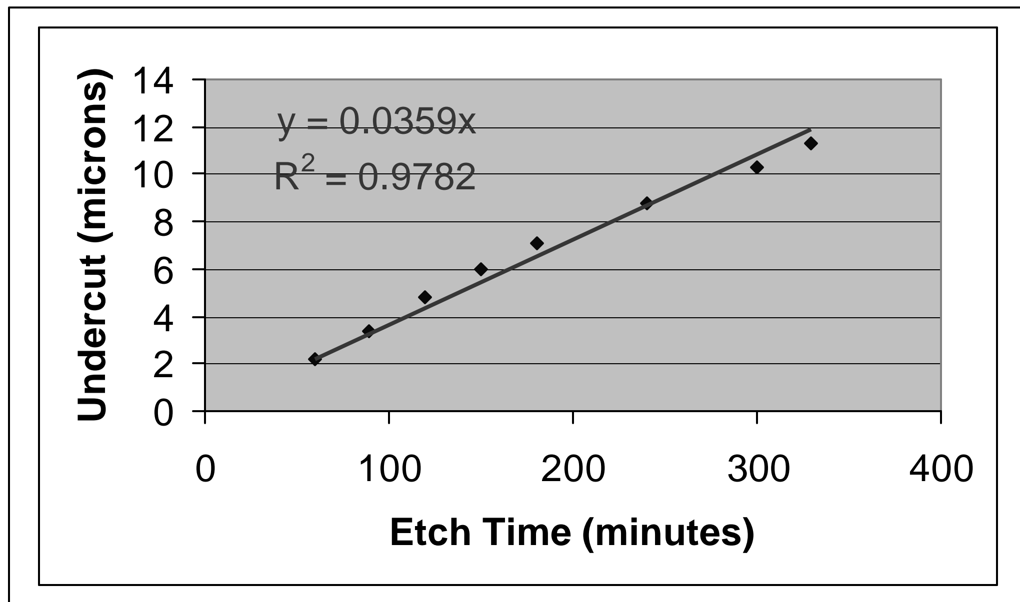

Figure 6: Polysilicon undercut through 10 micron features.

The lateral etch rate appears to be relatively linear with respect to time. A least-squares regression was constrained to force a y-intercept at zero, since no etch can occur prior to the initiation of the vapor delivery process. Short etch times were not evaluated since they are not applicable to the release etch we are targeting. It is known, however, that some non-linearity exists during the etch initiation. This is due to the fact that at t = 0, the concentration of HF vapor in the process chamber is zero. Since the chamber is not pressurized, flow out = flow in and the concentration in the chamber will increase over time, approaching a steady-state concentration within several minutes.

A specific test pattern of various sized vias was created in a thin polysilicon layer over an oxide layer. The sample was etched for a period of time and the amount of undercut was characterized in view of the diameter of the via. There was a definite correlation between the size of the via opening and the amount of undercut achieved, as shown in Figure 7, along with the results of the linear regression analysis which was performed.

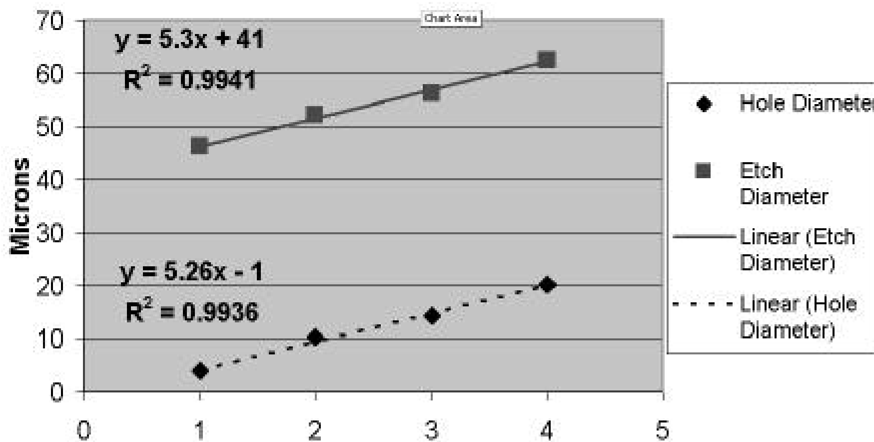

Figure 7: Correlation between contact hole diameter and undercut etch diameter

It is of interest to note that the slope of the lines in both cases is virtually identical, which would lead one to conclude that the amount of undercut is strongly influenced by the dimension through which the vapor must enter in order to access the release layer. This influence appears to be quite distinct. A 400% increase in the via dimension (from 5 microns to 20 microns) translates to a 35% increase in the amount of undercut (from 46 microns to 62 microns). This effect is further illustrated in Figure 8, which is an IR microscope image of the test pattern and the undercut.

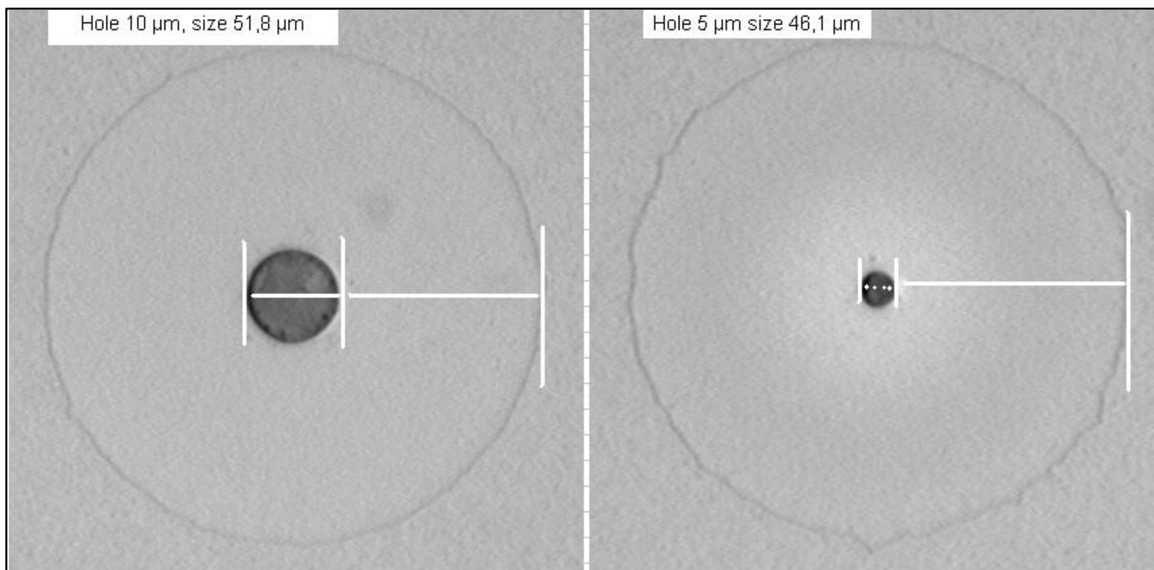

Figure 8: IR image of silicon membrane after HF vapor etch.

Release Etch:

Whether or not the correlation between device geometry and undercut is significant will depend largely on the device design. As with all MEMS designs, adequate consideration must be given so as to provide access for the etchant species, whatever it may be, to the release layer. Some designs incorporate a "hard stop" where an extreme amount of over-etch may be performed without device liability. Other designs rely on a specific amount of oxide remaining in order to support the moving structure, in which case a predictable undercut is essential to successful device fabrication. Figure 9 shows an IR image of a beam structure with specific attributes of the HF vapor etch highlighted.

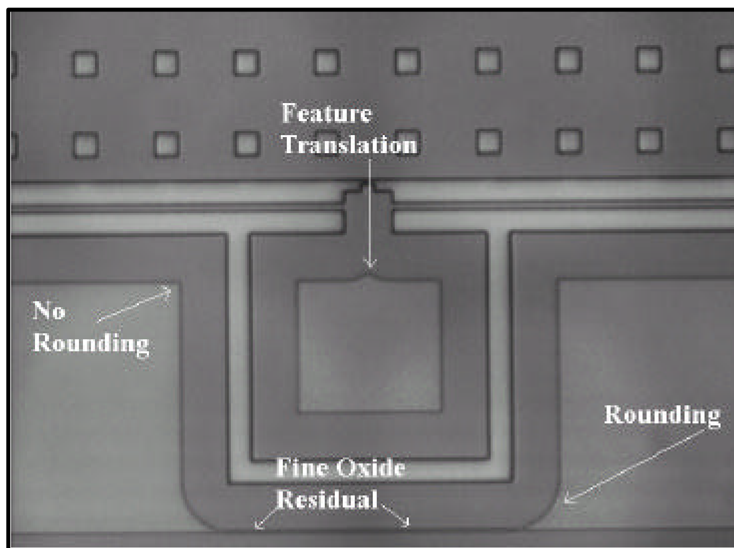

Figure 9: MEMS feature pattern translation to undercut

Several items are worth noting in regards to the HF Vapor etch of the accelerometer structure shown. Note that the anchor beam support feature is translated nicely into the residual oxide, indicating a very uniform amount of undercut. This is further emphasized by the corner features. Exterior corners are subject to an equidistant attack from each edge, therefore no rounding occurs and the intersecting edges remain perpendicular. Interior corners are slowly receding from the point of vapor diffusion, thus the apex of the curve is farthest from the point of vapor introduction to the undercut and the corner is rounded to a significant degree. Finally, at the bottom of the image we see a very fine line of residual oxide. The line is unbroken and uniform in width, again indicating uniform diffusion underneath the polysilicon device structure.

In additional IR images of the same accelerometer device are shown in Figure 10. Figure 10(a) shows an overview of the device structure. Figure 10(b), (c) and (d) give more detailed views of the device, specifically showing the undercut and the residual oxide which forms the support structure for the device. These continue to show the uniform undercut of the structure which was released without stiction.

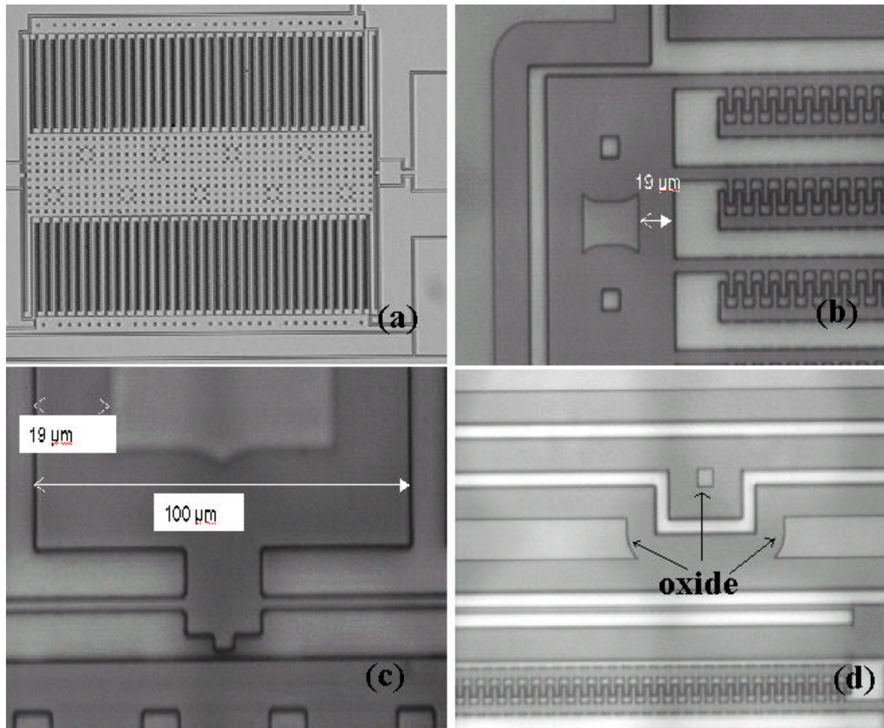

Figure 10: Accelerometer features released in HF vapor etch (a) accelerometer view (b) anchor fixed electrodes (c) anchor beam undercut (d) support residual

A three-dimensional view of an accelerometer structure is shown in Figure 11. In this particular device, the HF vapor first had to diffuse between the combs in the vertical plane approximately 75 microns. The distance between the silicon fingers was less than two microns and a five micron per side undercut was required to release the structure. The release layer was a one micron thick thermal oxide layer. Consistent release of the structures was achieved without stiction or degradation to device performance. It is of interest to note that electron charging of the structure caused repulsion of the structures followed by charge bleed-off, with the result being the visual verification of structure movement while observed in the SEM.

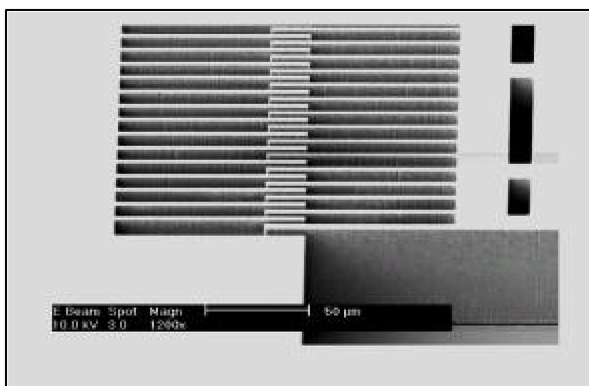

Figure 11: Three dimensional view of a released accelerometer finger structure

CONCLUSIONS

A batch HF vapor etch process has been characterized with regard to MEMS release etch applications. While the initial test apparatus showed a limitation in regards to oxide loading, etch uniformity and repeatability were acceptable as long as the amount of exposed oxide was less than 8835 cm2 in a given load. This is not seen to be a significant liability due to the fact that this may be circumvented by (a) backside oxide removal prior to the release etch, (b) bulk oxide removal prior to the release etch, (c) limiting the load size to not more than 13 200mm wafers or (d) installing a second HF vapor generator on the system, which is being incorporated in the current design. Metal ion contamination was tested using VPD ICP-MS, and showed no increase in metallic contaminants after processing. Particle performance was shown to be acceptable. The undercut of device features was repeatable and predictable. Most importantly, the system has been used to successfully release various accelerometer structures without stiction. Processing times and device performance have been similar to what has been achieved in single-wafer release etch platforms, but with the advantage of being able to greatly improve throughput due to the batch processing capabilities of the system, making the system attractive for high-volume production applications.

REFERENCES

(1) U.S. Patent 5,954,911 and U.S. Patent 6,319,841
(2) U.S. Patent 6,126,734