



PEAKS

Symposium on Electrochemical
Processes for Microelectronics

**June 24-27, 2008
Kalispell, Montana USA**

Call For Papers

ABSTRACTS DEADLINE: April 15, 2008

Submit one original, properly formatted abstract either electronically or on paper by April 15, 2008 to:

Semitool, Inc.
ATTN: Terri Kissane
655 West Reserve Drive
Kalispell, Montana 59901 USA
peaks@semitool.com
<http://www.semitool.com/peaks>

Peaks in Plating is soliciting abstracts on electrochemical processing for microelectronic applications. Abstracts should explicitly state objectives, new results, and conclusions or significance of the work. Some papers will be scheduled for poster presentation. All authors selected for either oral or poster presentations will be notified by April 25, 2008. Abstracts should be no more than one page in length, one inch left and right margins, and single-spaced. The title should be centered, capitalized, and in bold face. The preferred font is 10pt, Times New Roman. Type author(s), affiliation(s), and address(es) centered below the title.

PRESENTATIONS

All oral presentation materials must be submitted electronically no later than June 13, 2008. Formatting and submission instructions will be included with the acceptance notification.

Oral presentations must be in English. An LCD projector and laptop with a CD-ROM drive will be available for PowerPoint presentations. Presenters who prefer to use their own laptops should verify laptop/projector compatibility prior to their presentation. Speakers requiring additional equipment must make a request prior to June 20, 2008.

Poster presentations will be displayed in English on a board approximately 4 feet high by 3 feet wide (1.22 meters high by .91 meters wide).

PUBLICATION

All papers and presentations will be available on CD. CDs will be distributed to all seminar attendees at no extra charge.

SUBJECTS OF INTEREST

- ❑ **Copper Interconnect ECD Processes:** Chemistry, Processes and Copper Interconnect Structures and Properties
- ❑ **Electroless Deposition:** Selective Barrier Capping, Packaging Processes, Process Stability And Control
- ❑ **ECD Alloy Deposition:** Electroless And Electrolytic Alloy Deposition, Magnetic Alloys, Solder Alloy Processes
- ❑ **Properties Of Electrochemically Deposited Materials:** Stress, Crystallographic Texture, Mechanical Properties, Magnetic Properties And Their Relationship To Electrochemical Deposition Processes
- ❑ **Anodic Process:** Anodization To Form High-K Dielectric Materials, Electrochemical Etching, Electrophoretic Deposition
- ❑ **Chemical Analysis Of Electrolytes:** Electroanalytical Methods (CVS, PCGA, Etc.), Control Of Electrolyte Concentrations, Novel Analysis Methods, Measuring Additive Breakdown Products
- ❑ **Novel Applications Of Electrochemical Processing For Microelectronic Applications:** Packaging, MEMS, Micro-Component Technology, Thin Film Heads
- ❑ **Modeling Of Electrochemical Processes:** Fluid Flow, Potential Distributions, Reactor Scale, Feature Scale
- ❑ **Surface Electrochemistry:** Atomic Layer Epitaxy, Self-Assembled Monolayers, Organic Additive Functionality